Performance Analysis of Monolithic RF Transformers by Experimental Characterization

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Abstract **_Electrical performances of 4-port n:n dual-spiral transformers fabricated in a thick plated copper on silicon process are analyzed. Multiport data analysis techniques and compact modeling are used to study the relationships between the physical and the electrical attributes of the devices. Analytical models, based on measurements from 50MHz to 20GHz, are used to explore achievable device performance under different design constraints.**

I. INTRODUCTION

The recent application of transformers in integrated VCOs, LNAs, filters, power amplifiers and mixers demonstrates the potential value of this component for realizing future radio front-end transceivers for wireless communication. A systematic implementation of these solutions into commercial product lines, however, has been handicapped by the lack of sufficient knowledge on the performance characteristics of on-chip transformers. Most works reported in this area have been limited to optimimizing the transformers only for the designated applications because the available tools do not allow the RFIC designer to accurately predict the performance of the devices. The work in [1] discusses design guidelines for achieving targeted inductance and mutual coupling coefficients for on-chip transformers, but is based mostly on EM simulation.

This work addresses the dependence of the electrical performance (inductance, common mode rejection ratio, mutual coupling coefficient and parasitic capacitance) of transformers built on lossy silicon substrate on their geometrical attributes (line width, line spacing, inner diameter, number of turns per inductor). Since some applications require low mutual coupling coefficients (e.g. peaking coils of broadband amplifiers) [5] while others require high mutual coupling coefficient (e.g. interstage matching networks), a design of experiment (DOE) approach is used to explore a large design space of broad interest to the RFIC design community.

II. DEVICE TOPOLOGY AND FABRICATION

A top view of the dual-spiral transformer including measurement pads and surrounding ground is shown in Fig. 1. The topology is similar to that of the spiral Marchand balun described in [3]; however, the device here is laid out with special considerations that enable an easy identification of the center of each spiral. This is very important for differential designs where the center tap is used for DC biasing. A transformer, whose physical center coincides with its electrical center, has little imbalance and therefore contributes to lowering the overall power consumption of the circuit in which it is applied.

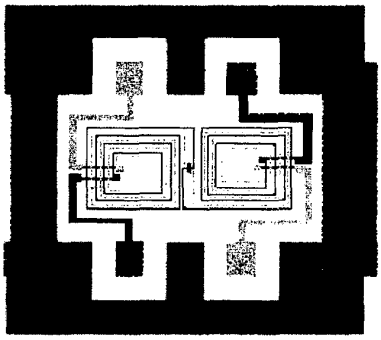

Fig. 1. Top view of a 4-port dual-spiral transformer

The transformer of Fig. 1 also has the advantage that the current flow in any two adjacent lines always has the same direction. This allows an enhanced positive mutual coupling between the two halves of each spiral as well as between the two spirals themselves. This topology is hence expected to provide mutual coupling coefficients at least as good as the best values reported to date for planar on-chip transformers. Finally, laying out the transformer as a four-port structure makes it possible to capture some of the parasitics that a two-port topology would not allow. The transformers were fabricated on the top most layer of a 4-metal level BiCMOS process using 18 Ohm-cm silicon as substrate and 10um thick copper for the metallization lines. The next lower level was used exclusively for underpasses. The line width, line spacing, and inner diameter were varied within the process limits to cover a very large design space. More than 40 devices were fabricated and characterized.

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III. Laboratory Measurement

Standard four-port S-parameters of the transformers are measured from 50 MHz to 20 GHz in 50 MHz steps using an ATN multiport system and 150-microns pitch GSGSG (ground-signal-ground-signal-ground) air coplanar probes in a 50-Ohm environment. The effects of the pads on the measured data are removed by means of subtraction in the Y-parameter domain. The mixed-mode S-parameters are derived from the corrected standard S-parameters using the linear transformation described by [4]. The relationship between the standard four-port S-parameters (S^{std}) and the mixed-mode S-parameters (S^{mm}) is given by

$$S^{std} = M^{-1} \cdot S^{mm} \cdot M \tag{1}$$

Where

$$S^{std} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix} \tag{2}$$

$$S^{mm} = \begin{bmatrix} S_{dd11} & S_{dd12} & S_{dc11} & S_{dc12} \\ S_{dd21} & S_{dd22} & S_{dc21} & S_{dc22} \\ S_{cd11} & S_{cd12} & S_{cc11} & S_{cc12} \\ S_{cd21} & S_{cd22} & S_{cc21} & S_{cc22} \end{bmatrix} \tag{3}$$

$$M = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix}$$

The mixed-mode S-parameter matrix S^{mm} (3) can be divided into 4 different 2-by-2 S-parameters matrices S_{dd}, S_{dc}, S_{cd} and S_{cc}, which represents the four possible modes of operation for a 4-port device. The indices dd, dc, cd and cc stand for differential mode to differential mode, differential mode to common mode, common mode to differential mode and common mode to common mode of operations, respectively.

IV. Electrical Measures of Performance of On-chip Transformers

Electrical measures of performance for on-chip transformers can be grouped into two classes: The first class includes parameters such as the insertion loss, the magnitude and phase imbalances, and the common mode rejection ratio, which can be extracted directly from measured S-, Y- and Z-parameters. The second category includes parameters such as the series inductance of the primary and secondary, the mutual coupling coefficient, and the parasitic capacitances and resistances, which until now could only be extracted through indirect means such as compact modeling.

A. Measurable Electrical Attributes

Most measurable performance metrics for on-chip transformers can be obtained directly from mixed-mode S-parameters.

The insertion loss (IL) represents the fraction of power transmitted from the primary to the secondary (S21) in the differential-to-differential mode of operation. The dependence of IL on the number of turns and the inner diameter was discussed in [2]. Its dependence on the line width and line spacing, as illustrated in Fig. 2, shows that it decreases with increasing line width and line spacing. In fact, increasing the line width increases the capacitive coupling between the two inductors and with it the transmitted common mode signal.

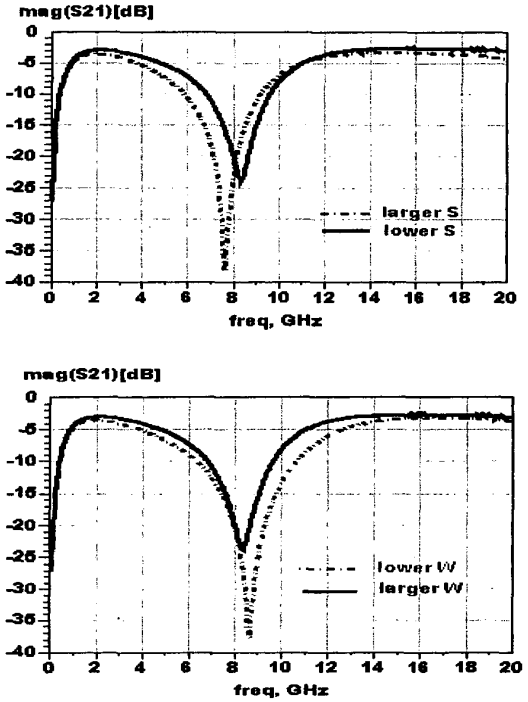

Fig. 2. Measured insertion loss vs line spacing (S) (top) and line width (W) (bottom)

The imbalances are quantified through the differential-to-ommon and common-to-differential terms of the mixed mode S-parameters, also called mode conversion terms. A well-balanced device exhibits no mode conversion.

The common mode rejection ratio (CMRR) is the differential-to-differential to common-to-common mode signal ratio. It is described by

$$CMRR = 10 \cdot \log\left(S_{dd21} / S_{cc21}\right) \qquad (4)$$

The CMRR decreases with line width and increases with the inner diameter. It's behavior over frequency is similar to that of the IL.

B. Analytical Model Development Process

The development process of an analytical model involves three major steps.

First, a compact model form is defined and the measured 4-port S-parameters of each device are fitted using a numerical simulation tool such. The compact model form of Fig. 3 is used in this work. As reported previously in [2], this model has the advantage that it is a true 4-port model and will work for transformers in configurations involving lower numbers of ports (e.g. three-port single ended, 2-port differential-to-differential, 2-port common mode to common mode, etc.).

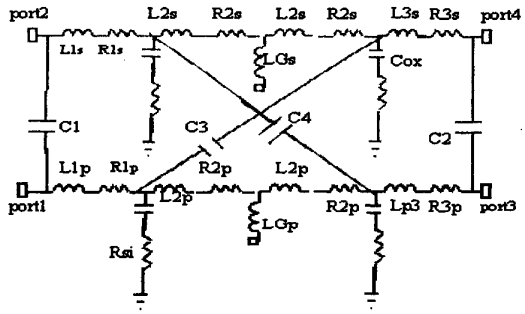

Fig. 3. Compact model of a 4-port on-chip transformer

Second, the extracted parameters are used to compute well-known transformer performance attributes. For example, the overall inductance of each inductor can be approximated as the sum of the individual series inductance, whereas the equivalent mutual coupling coefficient for each transformer is derived from the lumped element model using the voltage and current relationships for cascaded ideal transformers.

Third, analytical models, relating the physical parameters to the elements of the equivalent circuits, are developed using a statistical model analysis tool.

C. Modeling Results and Analysis

Fig. 4 shows the modeled vs. predicted inductance of the primary inductor. Fig. 5 and 6 are illustrations of the series inductance as function of the geometrical attributes. These curves that can be used as design guides for the given technology platform are generated from the analytical models.

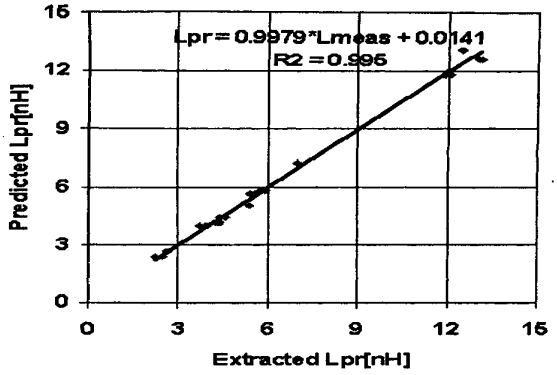

Fig. 4. Modeled vs. predicted total series inductance of the primary

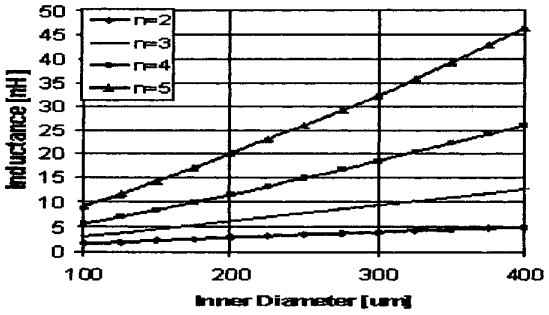

Fig. 5. Modeled inductance of secondary vs. inner diameter. Number of turns is used as parameter, W=S=6um

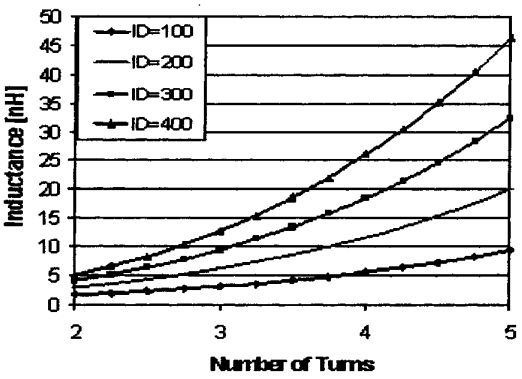

Fig. 6. Modeled inductance of the primary vs. number of turns. ID is used as parameter,W=S=6um

The developed model indicates that the mutual coupling coefficient is independent of the line width, but is strongly

dependent on the line spacing, number of turns and inner diameter. Small line spacing, large number of turns per inductor and large inner diameter are necessary to achieve large mutual coupling coefficient. Fig. 7 and 8 are illustrations of the achievable mutual couping coefficient under number of turns and inner diameter constraints respectively. The selected design space offers mutual coupling coefficients ranging from 0.4 to 0.85 for the selected device topology.

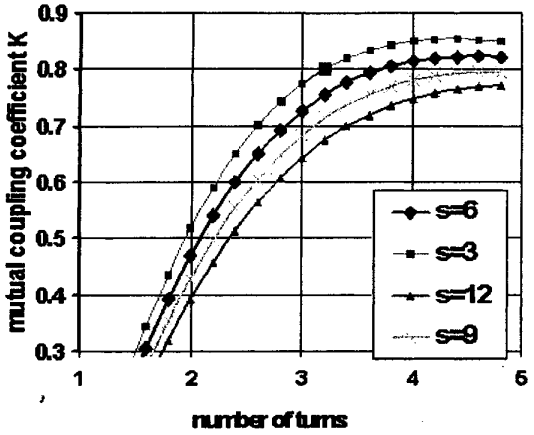

Fig. 7. Modeled mutual coupling coefficient vs. number of turns. The line spacing is used as parameter, ID=200um

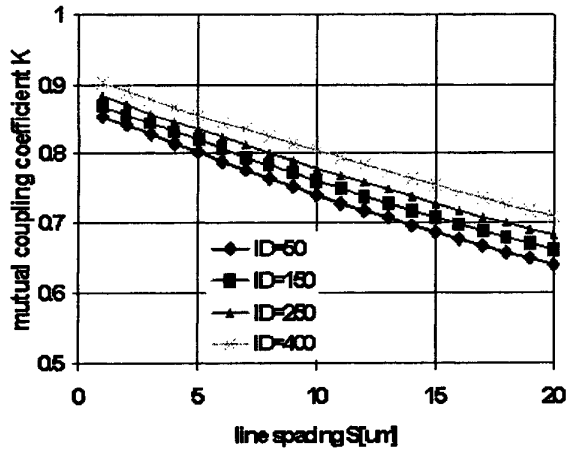

Fig. 8. Modeled mutual coupling coefficient vs. line spacing, ID[um] is used as parameter, N=4

V. CONCLUSION

Analytical models have been developed for four-port transformers fabricated on silicon using a thick plated copper process. These models, on one hand, can be used as fast predictive tools in place of electromagnetic simulation to accelerate the circuit design process. On the other hand they can also be used to study the limits of the current technology for transformer design as well the identification of process improvement necessary for better device performance.

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REFERENCES

[1] R. Long, "Monolithic transformers for silicon RF IC design", *IEEE Journal of Solid-Sate Circuits,* vol. 35, no. 9, Sept. 2000, pp. 1368-1382.

[2] T. Kamgaing, K. Zaki, T. Myers, M. Petras, M. Miller, "Full four-port modeling and characterization of spiral on-chip transformers for RFIC's", *proceedings of the 31st European Microwave Conference,* vol. 1, pp. 421-424, London, Sept. 2001

[3] K.S. Ang et al., " A compact MMIC balun using spiral transformers", *Microwave Conference, Asia Pacific,* pp. 655-658, 1999

[4] D.E. Bockelman and W.R. Eisenstadt, "Combined differential and common-mode scattering parameters: theory and simulation", *IEEE Trans. on Microwave Theory and Tech.,* Vol. 43, July 1995, pp. 1530 -1539

[5] T.H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits,* Cambridge University Press, 1998